National Semiconductor

June 23, 2008

# LMV793/LMV794 88 MHz, Low Noise, 1.8V CMOS Input, Decompensated Operational Amplifiers

## General Description

The LMV793 (single) and the LMV794 (dual) CMOS input operational amplifiers offer a low input voltage noise density of 5.8 nV/√Hz while consuming only 1.15 mA (LMV793) of quiescent current. The LMV793/LMV794 are stable at a gain of 10 and have a gain bandwidth product (GBW) of 88 MHz. The LMV793/LMV794 have a supply voltage range of 1.8V to 5.5V and can operate from a single supply. The LMV793/LMV794 each feature a rail-to-rail output stage capable of driving a 600Ω load and sourcing as much as 60 mA of current.

The LMV793/LMV794 provide optimal performance in low voltage and low noise systems. A CMOS input stage, with typical input bias currents in the range of a few femto-Amperes, and an input common mode voltage range, which includes ground, make the LMV793/LMV794 ideal for low power sensor applications where high speeds are needed.

The LMV793/LMV794 are manufactured using National's advanced VIP50 process. The LMV793 is offered in either a 5-Pin SOT23 or an 8-Pin SOIC package. The LMV794 is offered in either the 8-Pin SOIC or the 8-Pin MSOP.

## Features

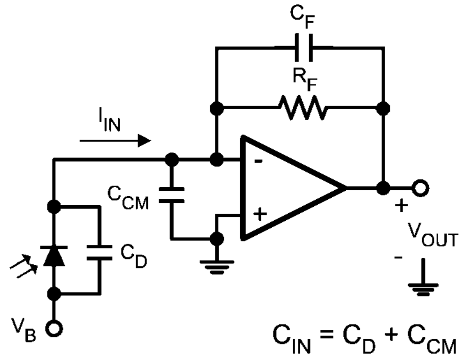
(Typical 5V supply, unless otherwise noted)

| | |
|---|---|
| ■ Input referred voltage noise | 5.8 nV/√Hz |
| ■ Input bias current | 100 fA |
| ■ Gain bandwidth product | 88 MHz |
| ■ Supply current per channel | |
| — LMV793 | 1.15 mA |
| — LMV794 | 1.30 mA |
| ■ Rail-to-rail output swing | |
| — @ 10 kΩ load | 25 mV from rail |
| — @ 2 kΩ load | 45 mV from rail |
| ■ Guaranteed 2.5V and 5.0V performance | |
| ■ Total harmonic distortion | 0.04% @1 kHz, 600Ω |
| ■ Temperature range | −40°C to 125°C |

## Applications

- ADC interface
- Photodiode amplifiers
- Active filters and buffers
- Low noise signal processing
- Medical instrumentation
- Sensor interface applications

## Typical Application

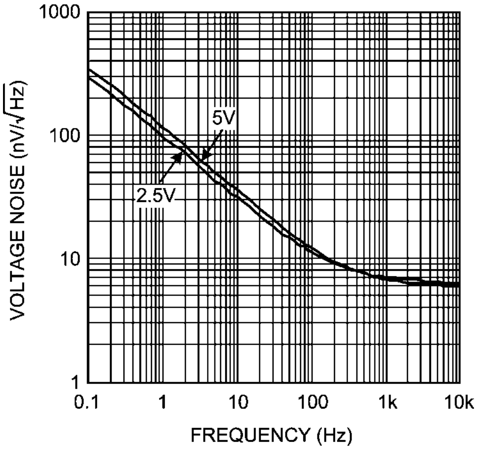


$$C_{IN} = C_D + C_{CM}$$

$$\frac{V_{OUT}}{I_{IN}} = - R_F$$

20216369

**Photodiode Transimpedance Amplifier**



20216339

**Input Referred Voltage Noise vs. Frequency**

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| ESD Tolerance (Note 2) | |
| Human Body Model | 2000V |
| Machine Model | 200V |
| Charge-Device Model | 1000V |
| $V_{IN}$ Differential | ±0.3V |
| Supply Voltage ($V^+ - V^-$) | 6.0V |
| Input/Output Pin Voltage | $V^+$ +0.3V, $V^-$ −0.3V |
| Storage Temperature Range | −65°C to 150°C |
| Junction Temperature (Note 3) | +150°C |
| Soldering Information | |
| Infrared or Convection (20 sec) | 235°C |
| Wave Soldering Lead Temp (10 sec) | 260°C |

## Operating Ratings (Note 1)

| | |
|---|---|
| Temperature Range (Note 3) | −40°C to 125°C |
| Supply Voltage ($V^+ - V^-$) | |
| $-40°C \le T_A \le 125°C$ | 2.0V to 5.5V |
| $0°C \le T_A \le 125°C$ | 1.8V to 5.5V |
| Package Thermal Resistance ($\theta_{JA}$ (Note 3)) | |
| 5-Pin SOT-23 | 180°C/W |
| 8-Pin SOIC | 190°C/W |
| 8-Pin MSOP | 236°C/W |

## 2.5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for $T_A = 25°C$, $V^+ = 2.5V$, $V^- = 0V$, $V_{CM} = V^+/2 = V_O$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | | | 0.1 | ±1.35<br>**±1.65** | mV |
| TC $V_{OS}$ | Input Offset Voltage Temperature Drift (Note 7) | LMV793 | | | −1.0 | | μV/°C |
| | | LMV794 | | | −1.8 | | |
| $I_B$ | Input Bias Current | $V_{CM} = 1.0V$ (Notes 8, 9) | $-40°C \le T_A \le 85°C$ | | 0.05 | 1<br>**25** | pA |
| | | | $-40°C \le T_A \le 125°C$ | | 0.05 | 1<br>**100** | |
| $I_{OS}$ | Input Offset Current | $V_{CM} = 1.0V$ (Note 9) | | | 10 | | fA |
| CMRR | Common Mode Rejection Ratio | $0V \le V_{CM} \le 1.4V$ | | 80<br>**75** | 94 | | dB |
| PSRR | Power Supply Rejection Ratio | $2.0V \le V^+ \le 5.5V$, $V_{CM} = 0V$ | | 80<br>**75** | 100 | | dB |
| | | $1.8V \le V^+ \le 5.5V$, $V_{CM} = 0V$ | | 80 | 98 | | |
| CMVR | Common Mode Voltage Range | CMRR ≥ 60 dB<br>CMRR ≥ 55 dB | | −0.3<br>**-0.3** | | 1.5<br>**1.5** | V |
| $A_{VOL}$ | Open Loop Voltage Gain | $V_{OUT} = 0.15V$ to 2.2V, $R_L = 2\ k\Omega$ to $V^+/2$ | LMV793 | 85<br>**80** | 98 | | dB |
| | | | LMV794 | 82<br>**78** | 92 | | |
| | | $V_{OUT} = 0.15V$ to 2.2V, $R_L = 10\ k\Omega$ to $V^+/2$ | | 88<br>**84** | 110 | | |
| $V_{OUT}$ | Output Voltage Swing High | $R_L = 2\ k\Omega$ to $V^+/2$ | | | 25 | 75<br>**82** | mV from either rail |
| | | $R_L = 10\ k\Omega$ to $V^+/2$ | | | 20 | 65<br>**71** | |
| | Output Voltage Swing Low | $R_L = 2\ k\Omega$ to $V^+/2$ | | | 30 | 75<br>**78** | |
| | | $R_L = 10\ k\Omega$ to $V^+/2$ | | | 15 | 65<br>**67** | |

| Symbol | Parameter | Conditions | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|---|---|---|---|---|---|---|
| $I_{OUT}$ | Output Current | Sourcing to $V^-$<br>$V_{IN}$ = 200 mV (Note 10) | 35<br>**28** | 47 | | mA |
| | | Sinking to $V^+$<br>$V_{IN}$ = –200 mV (Note 10) | 7<br>**5** | 15 | | |
| $I_S$ | Supply Current Per Amplifier | LMV793 | | 0.95 | 1.30<br>**1.65** | mA |
| | | LMV794 | | 1.1 | 1.50<br>**1.85** | |
| SR | Slew Rate | $A_V$ = +10, Rising (10% to 90%) | | 32 | | V/µs |
| | | $A_V$ = +10, Falling (90% to 10%) | | 24 | | |
| GBW | Gain Bandwidth | $A_V$ = +10, $R_L$ = 10 kΩ | | 88 | | MHz |
| $e_n$ | Input Referred Voltage Noise Density | f = 1 kHz | | 6.2 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input Referred Current Noise Density | f = 1 kHz | | 0.01 | | $pA/\sqrt{Hz}$ |
| THD+N | Total Harmonic Distortion + Noise | f = 1 kHz, $A_V$ = 1, $R_L$ = 600Ω | | 0.01 | | % |

## 5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for $T_A$ = 25°C, $V^+$ = 5V, $V^-$ = 0V, $V_{CM}$ = $V^+/2$ = $V_O$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | | | 0.1 | ±1.35<br>**±1.65** | mV |
| TC $V_{OS}$ | Input Offset Voltage Temperature Drift (Note 7) | LMV793 | | | –1.0 | | µV/°C |
| | | LMV794 | | | –1.8 | | |
| $I_B$ | Input Bias Current | $V_{CM}$ = 2.0V (Notes 8, 9) | –40°C ≤ $T_A$ ≤ 85°C | | 0.1 | 1<br>**25** | pA |
| | | | –40°C ≤ $T_A$ ≤ 125°C | | 0.1 | 1<br>**100** | |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = 2.0V (Note 9) | | | 10 | | fA |
| CMRR | Common Mode Rejection Ratio | 0V ≤ $V_{CM}$ ≤ 3.7V | | 80<br>**75** | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | 2.0V ≤ $V^+$ ≤ 5.5V, $V_{CM}$ = 0V | | 80<br>**75** | 100 | | dB |
| | | 1.8V ≤ $V^+$ ≤ 5.5V, $V_{CM}$ = 0V | | 80 | 98 | | |
| CMVR | Common Mode Voltage Range | CMRR ≥ 60 dB<br>CMRR ≥ 55 dB | | –0.3<br>**-0.3** | | 4<br>**4** | V |
| $A_{VOL}$ | Open Loop Voltage Gain | $V_{OUT}$ = 0.3V to 4.7V, $R_L$ = 2 kΩ to $V^+/2$ | LMV793 | 85<br>**80** | 97 | | dB |
| | | | LMV794 | 82<br>**78** | 89 | | |
| | | $V_{OUT}$ = 0.3V to 4.7V, $R_L$ = 10 kΩ to $V^+/2$ | | 88<br>**84** | 110 | | |

| Symbol | Parameter | Conditions | | Min (Note 6) | Typ (Note 5) | Max (Note 6) | Units |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output Voltage Swing High | $R_L$ = 2 kΩ to $V^+$/2 | LMV793 | | 35 | 75<br>**82** | mV from either rail |
| | | | LMV794 | | 35 | 75<br>**82** | |
| | | $R_L$ = 10 kΩ to $V^+$/2 | | | 25 | 65<br>**71** | |
| | Output Voltage Swing Low | $R_L$ = 2 kΩ to $V^+$/2 | LMV793 | | 42 | 75<br>**78** | |
| | | | LMV794 | | 45 | 80<br>**83** | |
| | | $R_L$ = 10 kΩ to $V^+$/2 | | | 20 | 65<br>**67** | |
| $I_{OUT}$ | Output Current | Sourcing to $V^-$<br>$V_{IN}$ = 200 mV (Note 10) | | 45<br>**37** | 60 | | mA |
| | | Sinking to $V^+$<br>$V_{IN}$ = –200 mV (Note 10) | | 10<br>**6** | 21 | | |
| $I_S$ | Supply Current per Amplifier | LMV793 | | | 1.15 | 1.40<br>**1.75** | mA |
| | | LMV794 per Channel | | | 1.30 | 1.70<br>**2.05** | |
| SR | Slew Rate | $A_V$ = +10, Rising (10% to 90%) | | | 35 | | V/µs |
| | | $A_V$ = +10, Falling (90% to 10%) | | | 28 | | |
| GBW | Gain Bandwidth | $A_V$ = +10, $R_L$ = 10 kΩ | | | 88 | | MHz |
| $e_n$ | Input Referred Voltage Noise Density | f = 1 kHz | | | 5.8 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input Referred Current Noise Density | f = 1 kHz | | | 0.01 | | $pA/\sqrt{Hz}$ |
| THD+N | Total Harmonic Distortion + Noise | f = 1 kHz, $A_V$ = 1, $R_L$ = 600Ω | | | 0.01 | | % |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

**Note 2:** Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

**Note 3:** The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

**Note 4:** Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

**Note 5:** Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

**Note 6:** Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the statistical quality control (SQC) method.

**Note 7:** Offset voltage average drift is determined by dividing the change in $V_{OS}$ by temperature change.

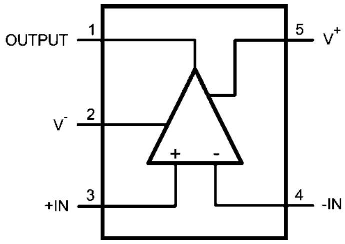
**Note 8:** Positive current corresponds to current flowing into the device.

**Note 9:** This parameter is guaranteed by design and/or characterization and is not tested in production.

**Note 10:** The short circuit test is a momentary test, the short circuit duration is 1.5 ms.

## Connection Diagrams

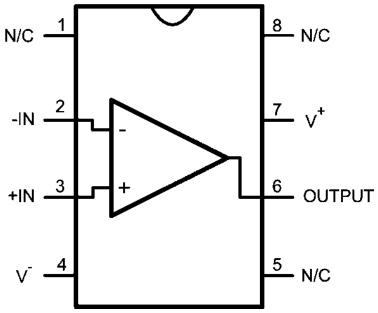
**5-Pin SOT-23 (LMV793)**



20216301

**Top View**

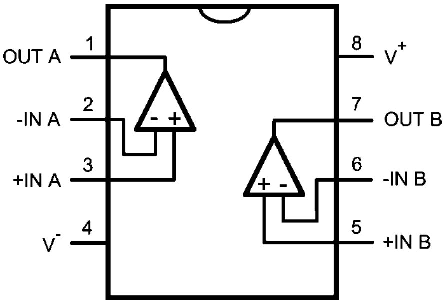
**8-Pin SOIC (LMV793)**



20216385

**Top View**

**8-Pin SOIC/MSOP (LMV794)**



20216302

**Top View**

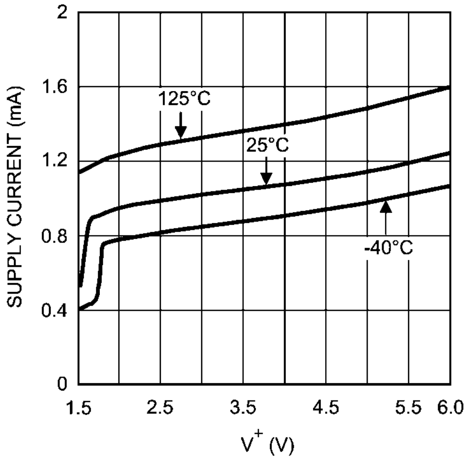
## Ordering Information

| Package | Part Number | Package Marking | Transport Media | NSC Drawing |
|---|---|---|---|---|
| 5-Pin SOT23 | LMV793MF | AS4A | 1k Units Tape and Reel | MF05A |
| | LMV793MFX | | 3k Units Tape and Reel | |
| 8-Pin SOIC | LMV793MA | LMV793MA | 95 Units/Rail | M08A |
| | LMV793MAX | | 2.5k Units Tape and Reel | |
| | LMV794MA | LMV794MA | 95 Units/Rail | |
| | LMV794MAX | | 2.5k Units Tape and Reel | |
| 8-Pin MSOP | LMV794MM | AN4A | 1k Units Tape and Reel | MUA08A |
| | LMV794MMX | | 3.5k Units Tape and Reel | |

## Typical Performance Characteristics

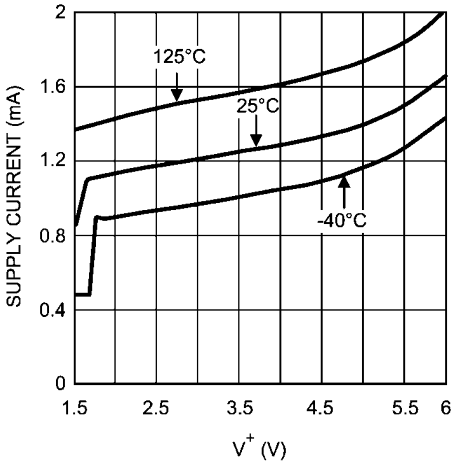
Unless otherwise specified, $T_A = 25°C$, $V^- = 0$, $V^+$ = Supply Voltage = 5V, $V_{CM} = V^+/2$.

### Supply Current vs. Supply Voltage (LMV793)



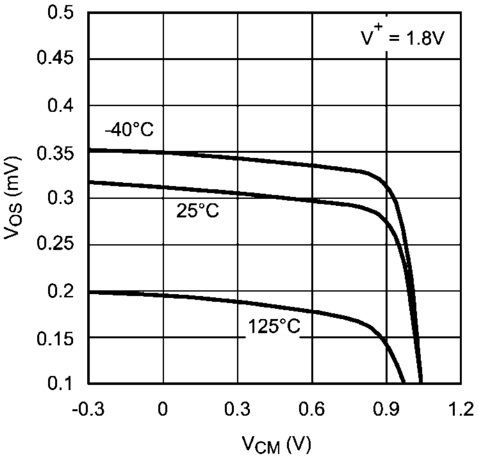
20216305

### Supply Current vs. Supply Voltage (LMV794)



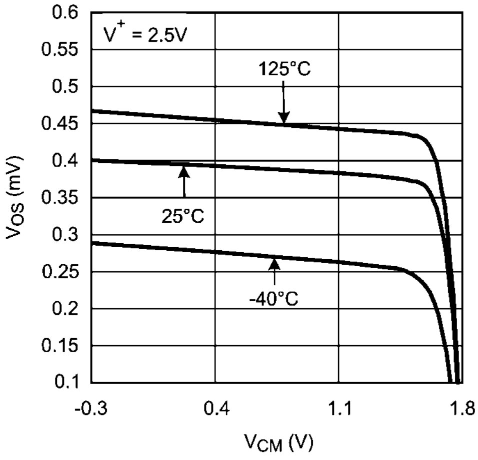
20216381

### $V_{OS}$ vs. $V_{CM}$



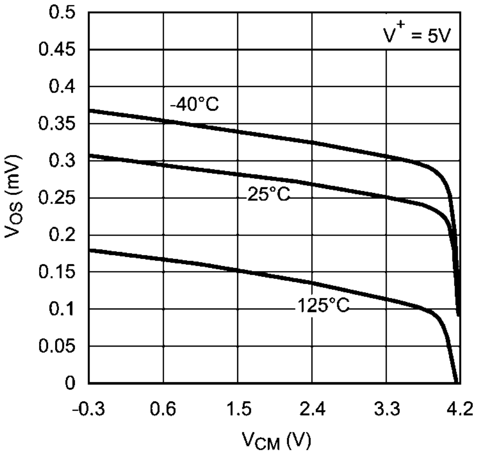
20216309

### $V_{OS}$ vs. $V_{CM}$



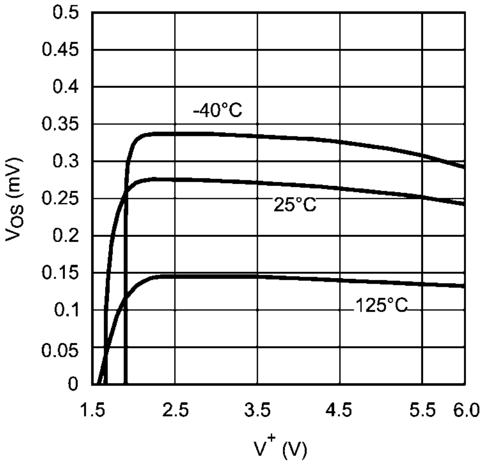
20216351

### $V_{OS}$ vs. $V_{CM}$



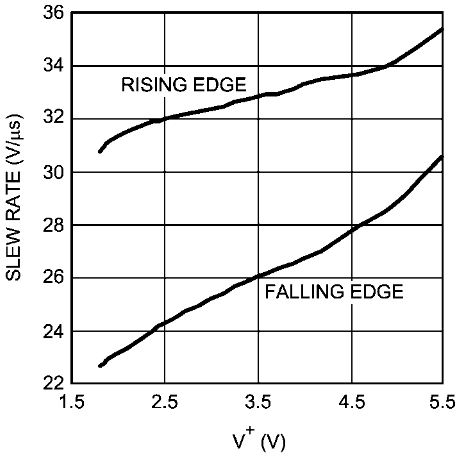
20216311

### $V_{OS}$ vs. Supply Voltage



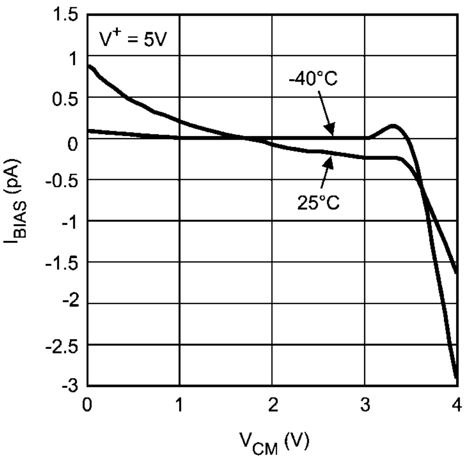
20216312

**Slew Rate vs. Supply Voltage**



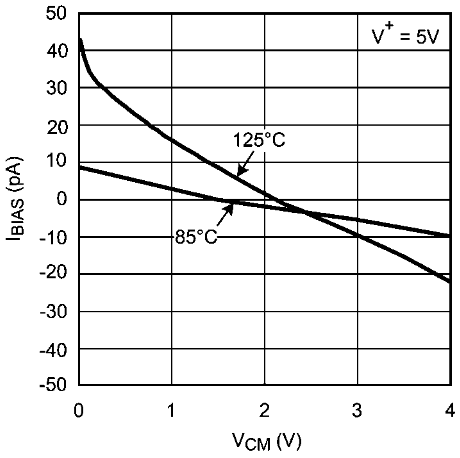
20216352

**Input Bias Current vs. $V_{CM}$**



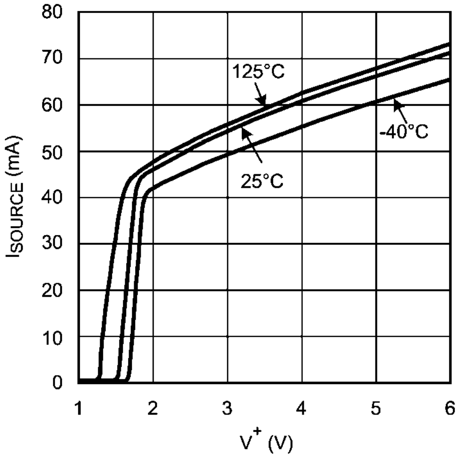
20216362

**Input Bias Current vs. $V_{CM}$**



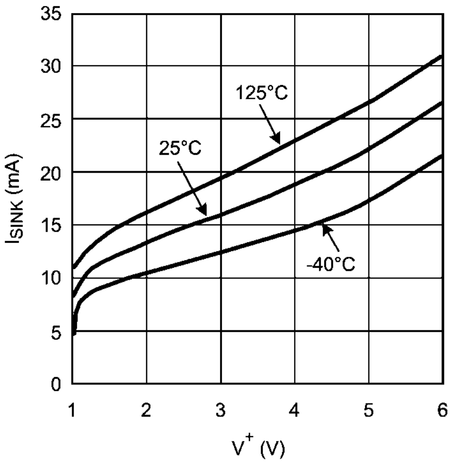
20216387

**Sourcing Current vs. Supply Voltage**



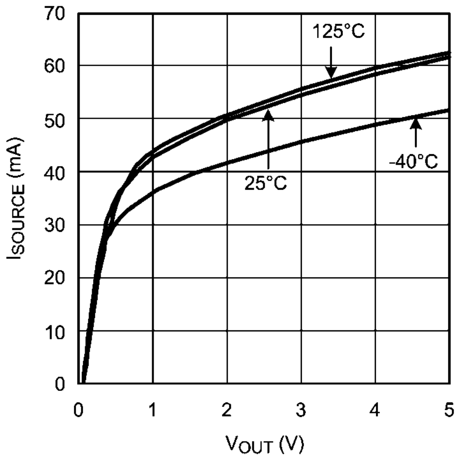
20216320

**Sinking Current vs. Supply Voltage**



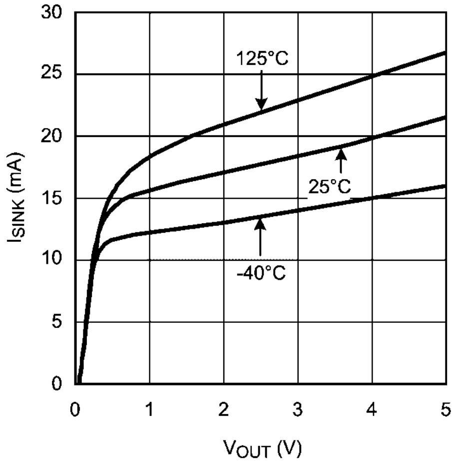
20216319

**Sourcing Current vs. Output Voltage**



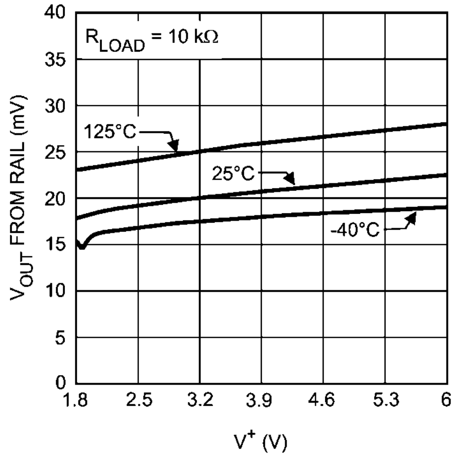
20216350

**Sinking Current vs. Output Voltage**



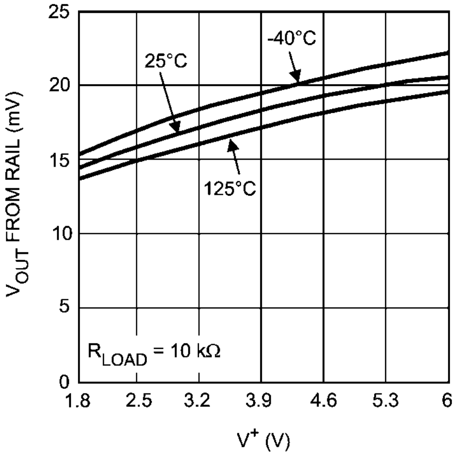
20216354

**Positive Output Swing vs. Supply Voltage**



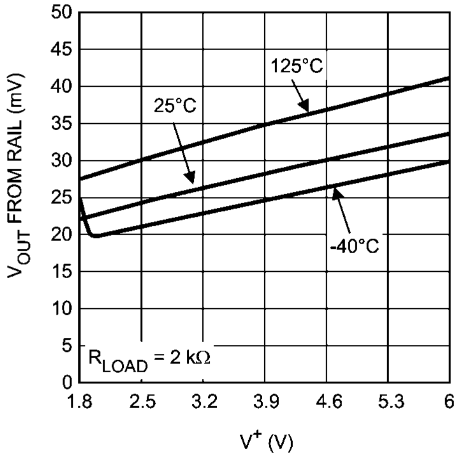
20216317

**Negative Output Swing vs. Supply Voltage**



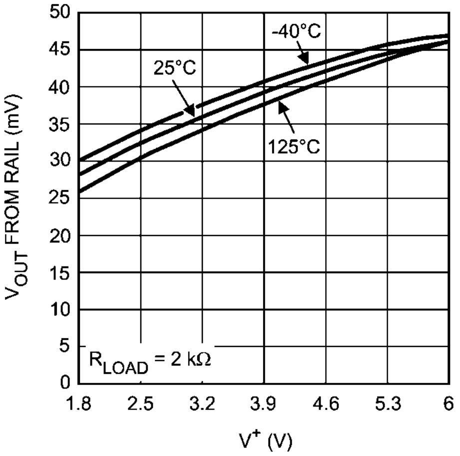
20216315

**Positive Output Swing vs. Supply Voltage**



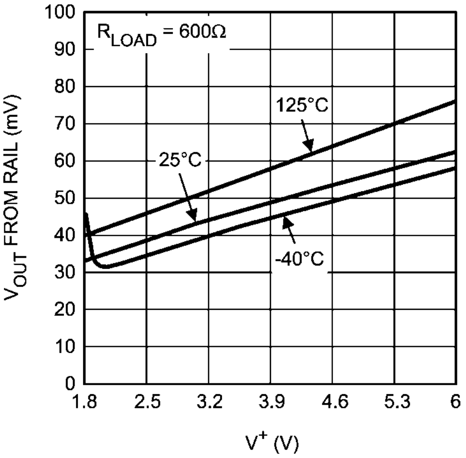
20216316

**Negative Output Swing vs. Supply Voltage**



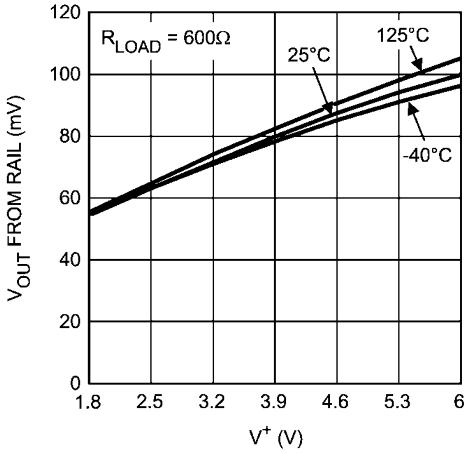
20216314

**Positive Output Swing vs. Supply Voltage**



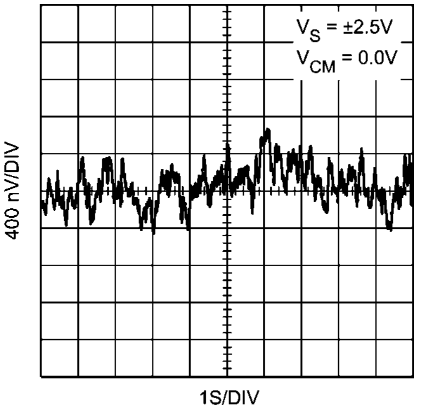
20216318

**Negative Output Swing vs. Supply Voltage**



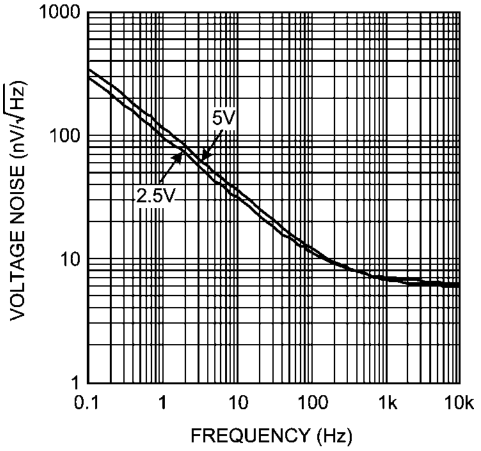
20216313

**Time Domain Voltage Noise**



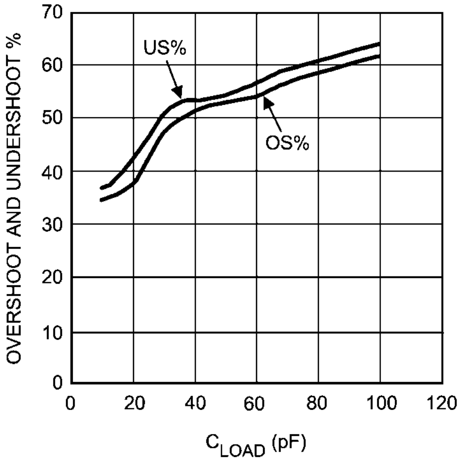
20216338

**Input Referred Voltage Noise vs. Frequency**



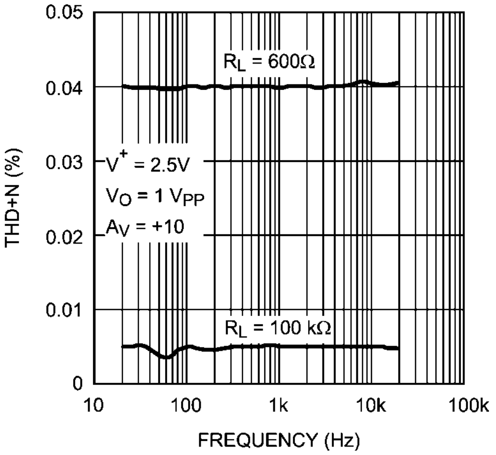
20216339

**Overshoot and Undershoot vs. $C_{LOAD}$**



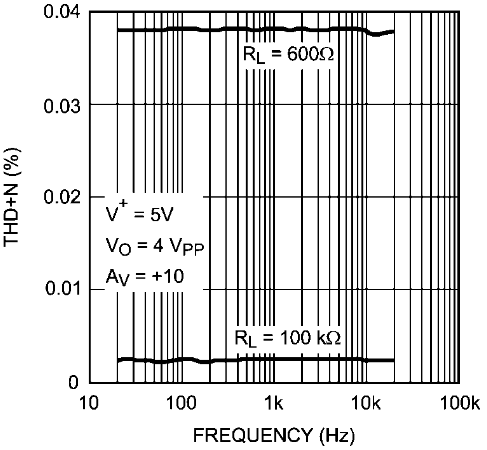
20216330

**THD+N vs. Frequency**



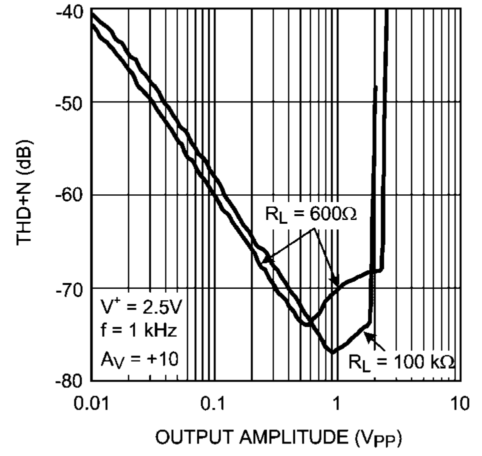
20216326

**THD+N vs. Frequency**



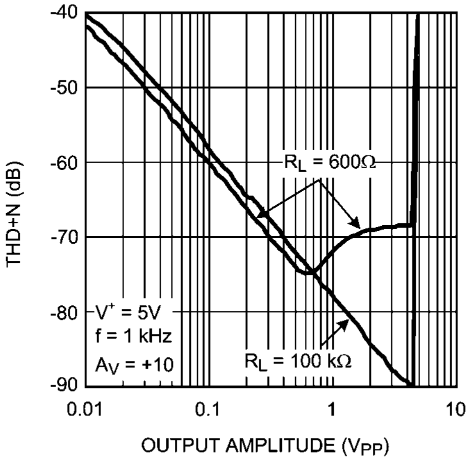
20216304

**THD+N vs. Peak-to-Peak Output Voltage ($V_{OUT}$)**



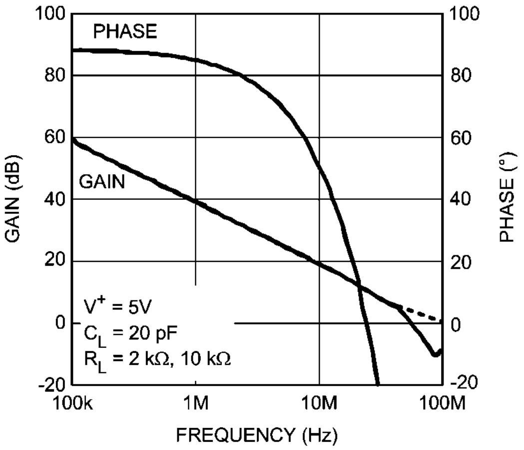
20216374

**THD+N vs. Peak-to-Peak Output Voltage ($V_{OUT}$)**



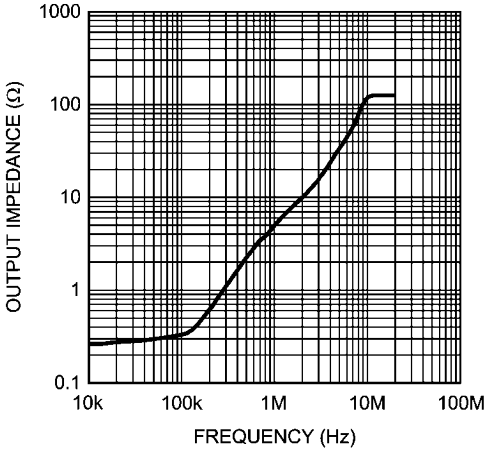
20216375

**Open Loop Gain and Phase**



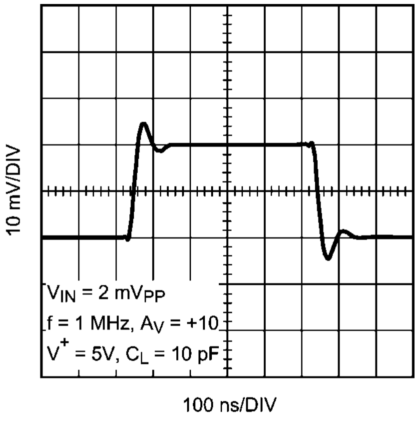
20216306

**Closed Loop Output Impedance vs. Frequency**



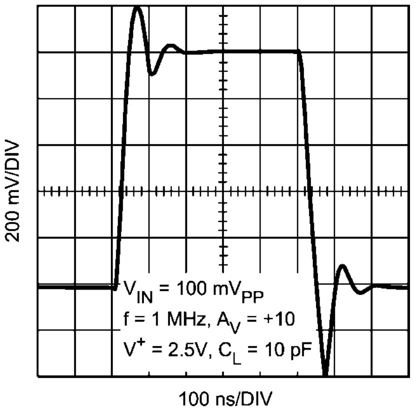
20216332

**Small Signal Transient Response, $A_V = +10$**



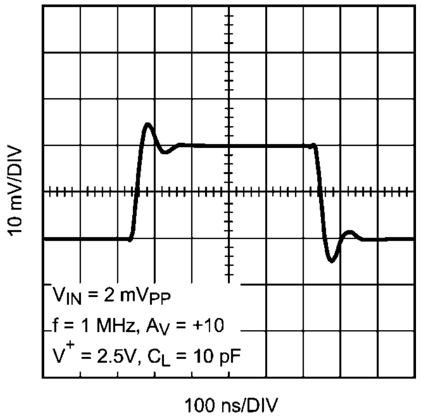
20216353

**Large Signal Transient Response, $A_V = +10$**



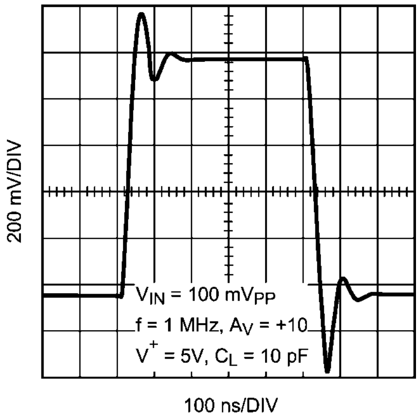
20216355

**Small Signal Transient Response, $A_V$ = +10**



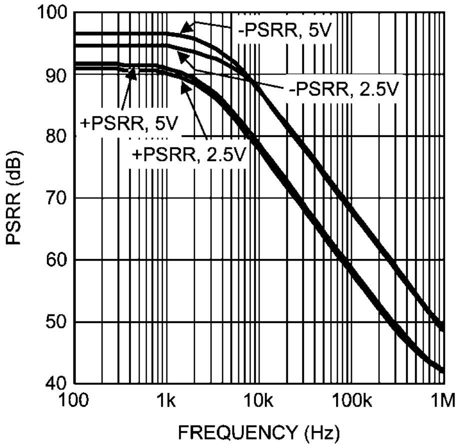
20216357

**Large Signal Transient Response, $A_V$ = +10**



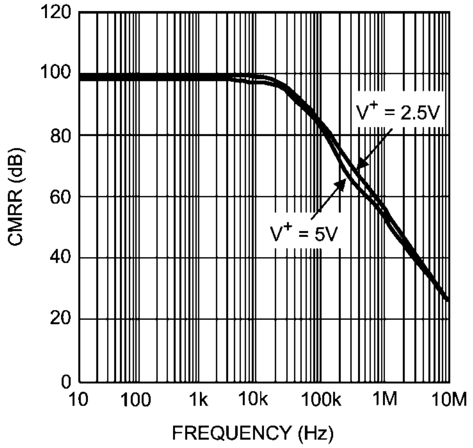
20216363

**PSRR vs. Frequency**



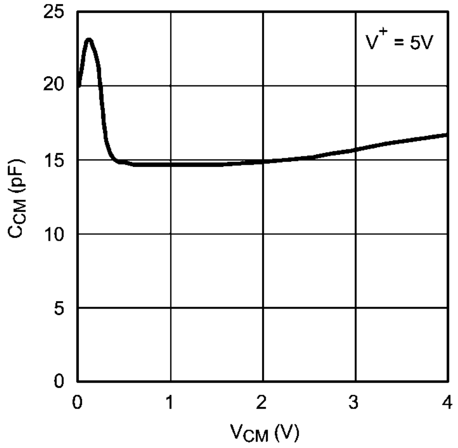
20216370

**CMRR vs. Frequency**



20216356

**Input Common Mode Capacitance vs. $V_{CM}$**



20216376

# Application Information

## ADVANTAGES OF THE LMV793/LMV794

### Wide Bandwidth at Low Supply Current

The LMV793/LMV794 are high performance op amps that provide a GBW of 88 MHz with a gain of 10 while drawing a low supply current of 1.15 mA. This makes them ideal for providing wideband amplification in data acquisition applications.

With the proper external compensation the LMV793/LMV794 can be operated at gains of ±1 and still maintain much faster slew rates than comparable unity gain stable amplifiers. The increase in bandwidth and slew rate is obtained without any additional power consumption over the LMV796.

### Low Input Referred Noise and Low Input Bias Current

The LMV793/LMV794 have a very low input referred voltage noise density (5.8 $nV/\sqrt{Hz}$ at 1 kHz). A CMOS input stage ensures a small input bias current (100 fA) and low input referred current noise (0.01 $pA/\sqrt{Hz}$). This is very helpful in maintaining signal integrity, and makes the LMV793/LMV794 ideal for audio and sensor based applications.

### Low Supply Voltage

The LMV793 and LMV794 have performance guaranteed at 2.5V and 5V supply. These parts are guaranteed to be operational at all supply voltages between 2.0V and 5.5V, for ambient temperatures ranging from –40°C to 125°C, thus utilizing the entire battery lifetime. The LMV793/LMV794 are also guaranteed to be operational at 1.8V supply voltage, for temperatures between 0°C and 125°C optimizing their usage in low-voltage applications.

### RRO and Ground Sensing

Rail-to-rail output swing provides the maximum possible dynamic range. This is particularly important when operating at low supply voltages. An innovative positive feedback scheme is used to boost the current drive capability of the output stage. This allows the LMV793/LMV794 to source more than 40 mA of current at 1.8V supply. This also limits the performance of these parts as comparators, and hence the usage of the LMV793 and the LMV794 in an open-loop configuration is not recommended. The input common-mode range includes the negative supply rail which allows direct sensing at ground in single supply operation.

### Small Size

The small footprint of the LMV793 and the LMV794 package saves space on printed circuit boards, and enables the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. Long traces between the signal source and the op amp make the signal path more susceptible to noise pick up.

The physically smaller LMV793/LMV794 packages, allow the op amp to be placed closer to the signal source, thus reducing noise pickup and maintaining signal integrity.

## USING THE DECOMPENSATED LMV793

### Advantages of Decompensated Op Amps

A unity gain stable op amp, which is fully compensated, is designed to operate with good stability down to gains of ±1. The large amount of compensation does provide an op amp that is relatively easy to use; however, a decompensated op amp is designed to maximize the bandwidth and slew rate without any additional power consumption. This can be very advantageous.

The LMV793/LMV794 require a gain of ±10 to be stable. However, with an external compensation network (a simple RC network) these parts can be stable with gains of ±1 and still maintain the higher slew rate. Looking at the Bode plots for the LMV793 and its closest equivalent unity gain stable op amp, the LMV796, one can clearly see the increased bandwidth of the LMV793. Both plots are taken with a parallel combination of 20 pF and 10 kΩ for the output load.

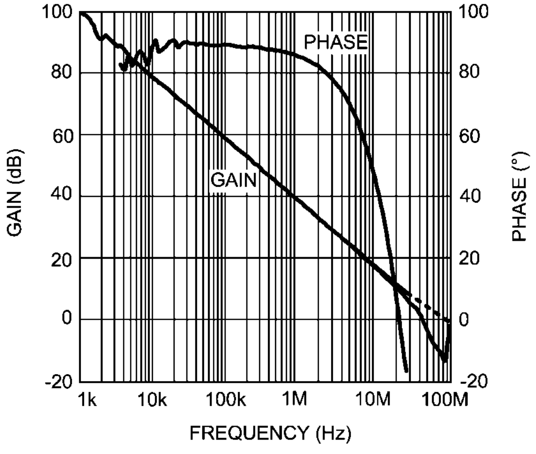


FIGURE 1. LMV793 $A_{VOL}$ vs. Frequency

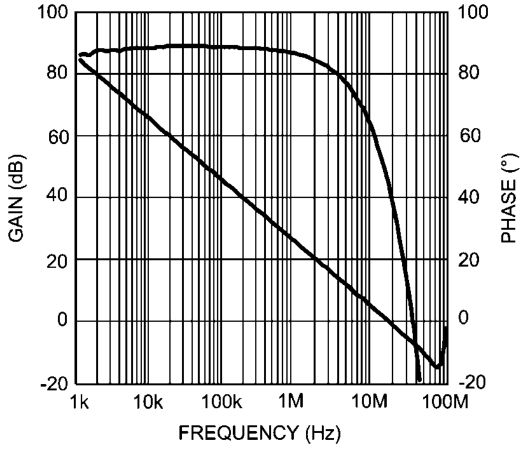


FIGURE 2. LMV796 $A_{VOL}$ vs. Frequency

*Figure 1* shows the much larger 88 MHz bandwidth of the LMV793 as compared to the 17 MHz bandwidth of the LMV796 shown in *Figure 2*. The decompensated LMV793 has five times the bandwidth of the LMV796.

### What is a Decompensated Op Amp?

The differences between the unity gain stable op amp and the decompensated op amp are shown in *Figure 3*. This Bode plot assumes an ideal two pole system. The dominant pole of the decompensated op amp is at a higher frequency, $f_1$, as compared to the unity-gain stable op amp which is at $f_d$ as shown in *Figure 3*. This is done in order to increase the speed capability of the op amp while maintaining the same power dissipation of the unity gain stable op amp. The LMV793/LMV794 have a dominant pole at 1.6 kHz. The unity gain stable LMV796/LMV797 have their dominant pole at 300 Hz.

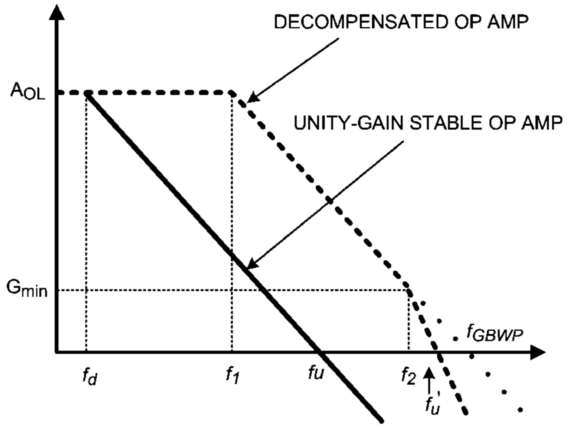


**FIGURE 3. Open Loop Gain for Unity-Gain Stable Op Amp and Decompensated Op Amp**

Having a higher frequency for the dominate pole will result in:

1. The DC open-loop gain ($A_{VOL}$) extending to a higher frequency.
2. A wider closed loop bandwidth.
3. Better slew rate due to reduced compensation capacitance within the op amp.

The second open loop pole ($f_2$) for the LMV793/LMV794 occurs at 45 MHz. The unity gain ($f_u$’) occurs after the second pole at 51 MHz. An ideal two pole system would give a phase margin of 45° at the location of the second pole. The LMV793/LMV794 have parasitic poles close to the second pole, giving a phase margin closer to 0°. Therefore it is necessary to operate the LMV793/LMV794 at a closed loop gain of 10 or higher, or to add external compensation in order to assure stability.

For the LMV796, the gain bandwidth product occurs at 17 MHz. The curve is constant from $f_d$ to $f_u$ which occurs before the second pole.

For the LMV793/LMV794, the GBW = 88 MHz and is constant between $f_1$ and $f_2$. The second pole at $f_2$ occurs before $A_{VOL}$ = 1. Therefore $f_u$’ occurs at 51 MHz, well before the GBW frequency of 88 MHz. For decompensated op amps the unity gain frequency and the GBW are no longer equal. $G_{min}$ is the minimum gain for stability and for the LMV793/LMV794 this is a gain of 18 to 20 dB.

### Input Lead-Lag Compensation

The recommended technique which allows the user to compensate the LMV793/LMV794 for stable operation at any gain is lead-lag compensation. The compensation components added to the circuit allow the user to shape the feedback function to make sure there is sufficient phase margin when the loop gain is as low as 0 dB and still maintain the advantages over the unity gain op amp. *Figure 4* shows the lead-lag configuration. Only $R_C$ and C are added for the necessary compensation.

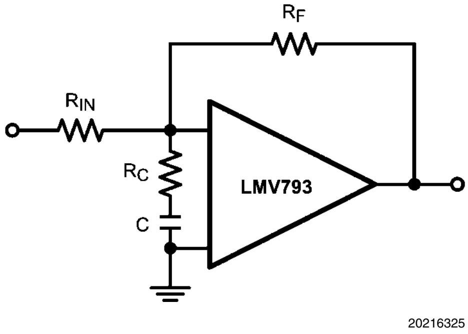


**FIGURE 4. LMV793 with Lead-Lag Compensation for Inverting Configuration**

To cover how to calculate the compensation network values it is necessary to introduce the term called the feedback factor or F. The feedback factor F is the feedback voltage $V_A$-$V_B$ across the op amp input terminals relative to the op amp output voltage $V_{OUT}$.

$$F = \frac{V_A - V_B}{V_{OUT}}$$

From feedback theory the classic form of the feedback equation for op amps is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + AF}$$

A is the open loop gain of the amplifier and AF is the loop gain. Both are highly important in analyzing op amps. Normally AF >>1 and so the above equation reduces to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{F}$$

Deriving the equations for the lead-lag compensation is beyond the scope of this datasheet. The derivation is based on the feedback equations that have just been covered. The inverse of feedback factor for the circuit in *Figure 4* is:

$$\frac{1}{F} = \left(1 + \frac{R_F}{R_{IN}}\right)\left(\frac{1 + s(R_c + R_{IN} \parallel R_F)\,C}{1 + sR_cC}\right) \tag{1}$$

where 1/F's pole is located at

$$f_p = \frac{1}{2\pi R_c C} \tag{2}$$

1/F's zero is located at

$$f_z = \frac{1}{2\pi(R_c + R_{IN} \parallel R_F)C} \tag{3}$$

$$\left.\frac{1}{F}\right|_{f=0} = 1 + \frac{R_F}{R_{IN}} \tag{4}$$

The circuit gain for *Figure 4* at low frequencies is $-R_F/R_{IN}$, but F, the feedback factor is not equal to the circuit gain. The feedback factor is derived from feedback theory and is the same for both inverting and non-inverting configurations. Yes, the feedback factor at low frequencies is equal to the gain for the non-inverting configuration.

$$\left.\frac{1}{F}\right|_{f=\infty} = \left(1+\frac{R_F}{R_{IN}}\right)\left(1+\frac{R_{IN} \,\|\, R_F}{R_C}\right) \qquad (5)$$

From this formula, we can see that

- 1/F's zero is located at a lower frequency compared with 1/F's pole.
- 1/F's value at low frequency is $1 + R_F/R_{IN}$.
- This method creates one additional pole and one additional zero.
- This pole-zero pair will serve two purposes:
  - — To raise the 1/F value at higher frequencies prior to its intercept with A, the open loop gain curve, in order to meet the $G_{min} = 10$ requirement. For the LMV793/ LMV794 some overcompensation will be necessary for good stability.
  - — To achieve the previous purpose above with no additional loop phase delay.

Please note the constraint $1/F \geq G_{min}$ needs to be satisfied only in the vicinity where the open loop gain A and 1/F intersect; 1/F can be shaped elsewhere as needed. The 1/F pole must occur before the intersection with the open loop gain A.

In order to have adequate phase margin, it is desirable to follow these two rules:

**Rule 1** 1/F and the open loop gain A should intersect at the frequency where there is a minimum of 45° of phase margin. When over-compensation is required the intersection point of A and 1/F is set at a frequency where the phase margin is above 45°, therefore increasing the stability of the circuit.

**Rule 2** 1/F's pole should be set at least one decade below the intersection with the open loop gain A in order to take advantage of the full 90° of phase lead brought by 1/F's pole which is F's zero. This ensures that the effect of the zero is fully neutralized when the 1/F and A plots intersect each other.

### Calculating Lead-Lag Compensation for LMV793/ LMV794

*Figure 5* is the same plot as *Figure 1*, but the $A_{VOL}$ and phase curves have been redrawn as smooth lines to more readily show the concepts covered, and to clearly show the key parameters used in the calculations for lead-lag compensation.

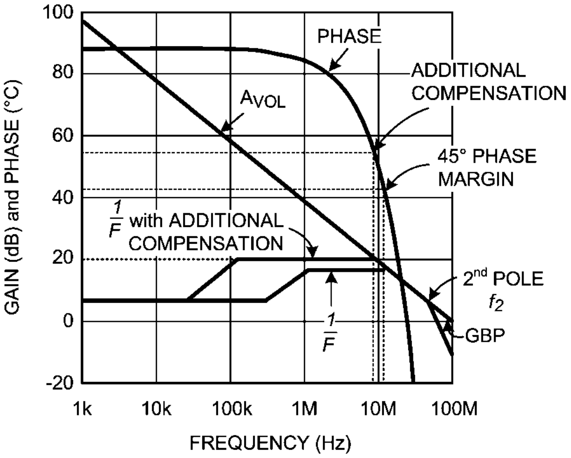


**FIGURE 5. LMV793/LMV794 Simplified Bode Plot**

To obtain stable operation with gains under 10 V/V the open loop gain margin must be reduced at high frequencies to where there is a 45° phase margin when the gain margin of the circuit with the external compensation is 0 dB. The pole and zero in F, the feedback factor, control the gain margin at the higher frequencies. The distance between F and $A_{VOL}$ is the gain margin; therefore, the unity gain point (0 dB) is where F crosses the $A_{VOL}$ curve.

For the example being used $R_{IN} = R_F$ for a gain of −1. Therefore F = 6 dB at low frequencies. At the higher frequencies the minimum value for F is 18 dB for 45° phase margin. From *Equation 5* we have the following relationship:

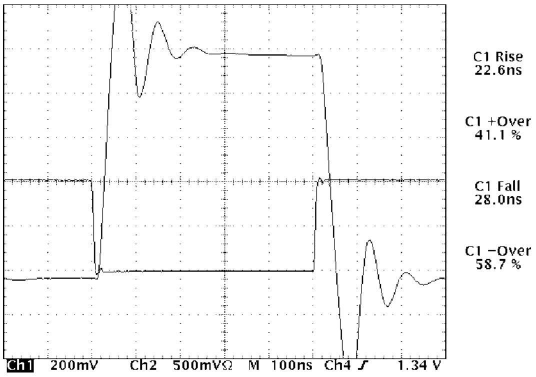
$$\left(1+\frac{R_F}{R_{IN}}\right)\left(1+\frac{R_{IN} \,\|\, R_F}{R_C}\right) = 18\text{ dB} = 7.9$$

Now set $R_F = R_{IN} = R$. With these values and solving for $R_C$ we have $R_C = R/5.9$. Note that the value of C does not affect the ratio between the resistors. Once the value of the resistors are set, then the position of the pole in F must be set. A 2 kΩ resistor is used for $R_F$ and $R_{IN}$ in this design. Therefore the value for $R_C$ is set at 330Ω, the closest standard value for 2 kΩ/5.9.

Rewriting *Equation 2* to solve for the minimum capacitor value gives the following equation:

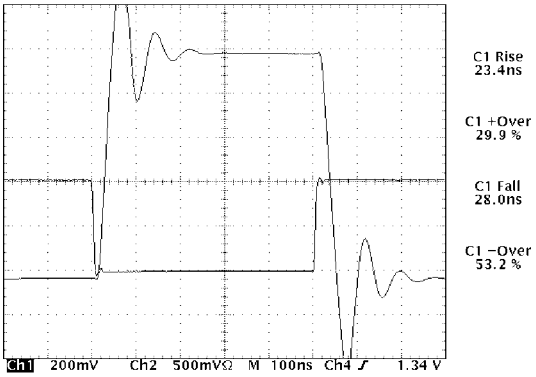
$$C = 1/(2\pi f_p R_C)$$

The feedback factor curve, F, intersects the $A_{VOL}$ curve at about 12 MHz. Therefore the pole of F should not be any larger than 1.2 MHz. Using this value and $R_c = 330\Omega$ the minimum value for C is 390 pF. *Figure 6* shows that there is too much overshoot, but the part is stable. Increasing C to 2.2 nF did not improve the ringing, as shown in *Figure 7*.



20216303

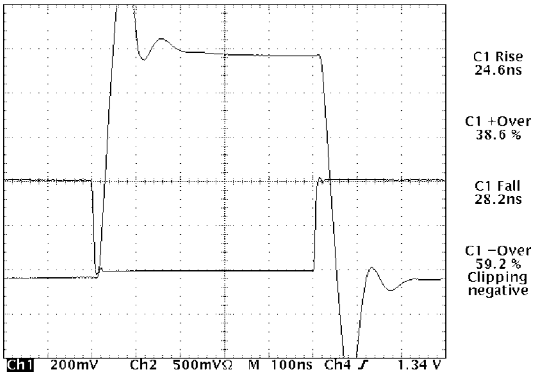
**FIGURE 6. First Try at Compensation, Gain = −1**



20216307

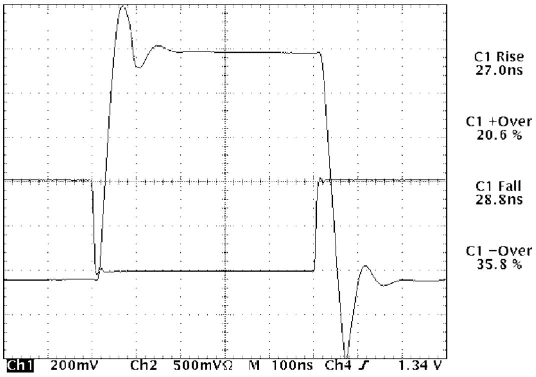
**FIGURE 7. C Increased to 2.2 nF, Gain = −1**

Some over-compensation appears to be needed for the desired overshoot characteristics. Instead of intersecting the $A_{VOL}$ curve at 18 dB, 2 dB of over-compensation will be used, and the $A_{VOL}$ curve will be intersected at 20 dB. Using *Equation 5* for 20 dB, or 10 V/V, the closest standard value of $R_C$ is 240Ω. The following two waveforms show the new resistor value with C = 390 pF and 2.2 nF. *Figure 9* shows the final compensation and a very good response for the 1 MHz square wave.



20216308

**FIGURE 8. $R_C$ = 240Ω and C = 390 pF, Gain = −1**



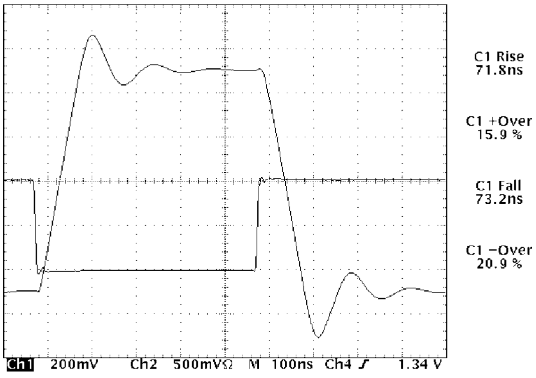
20216310

**FIGURE 9. $R_C$ = 240Ω and C = 2.2 nF, Gain = −1**

To summarize, the following steps were taken to compensate the LMV793 for a gain of −1:

1. Values for $R_c$ and C were calculated from the Bode plot to give an expected phase margin of 45°. The values were based on $R_{IN} = R_F$ = 2 kΩ. These calculations gave $R_c$ = 330Ω and C = 390 pF.
2. To reduce the ringing C was increased to 2.2 nF which moved the pole of F, the feedback factor, farther away from the $A_{VOL}$ curve.
3. There was still too much ringing so 2 dB of over-compensation was added to F. This was done by decreasing $R_C$ to 240Ω.

The LMV796 is the fully compensated part which is comparable to the LMV793. Using the LMV796 in the same setup, but removing the compensation network, provide the response shown in *Figure 10* .



20216321

**FIGURE 10. LMV796 Response**

For large signal response the rise and fall times are dominated by the slew rate of the op amps. Even though both parts are quite similar the LMV793 will give rise and fall times about 2.5 times faster than the LMV796. This is possible because the LMV793 is a decompensated op amp and even though it is being used at a gain of −1, the speed is preserved by using a good technique for external compensation.

### Non-Inverting Compensation

For the non-inverting amp the same theory applies for establishing the needed compensation. When setting the inverting configuration for a gain of −1, F has a value of 2. For the non-inverting configuration both F and the actual gain are the same, making the non-inverting configuration more difficult to compensate. Using the same circuit as shown in *Figure 4*, but setting up the circuit for non-inverting operation (gain of +2) results in similar performance as the inverting configuration with the inputs set to half the amplitude to compensate for the additional gain. *Figure 11* below shows the results.

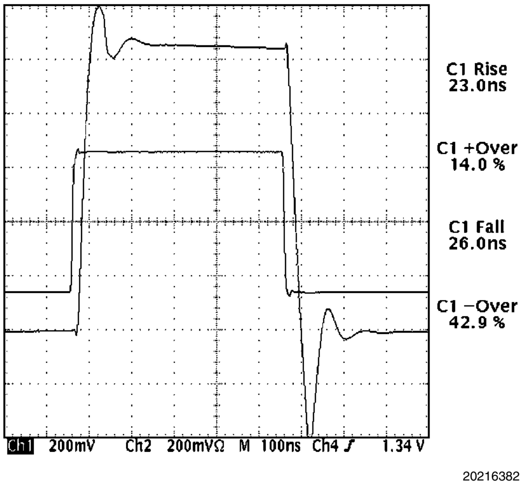


**FIGURE 11. $R_C$ = 240Ω and C = 2.2 nF, Gain = +2**

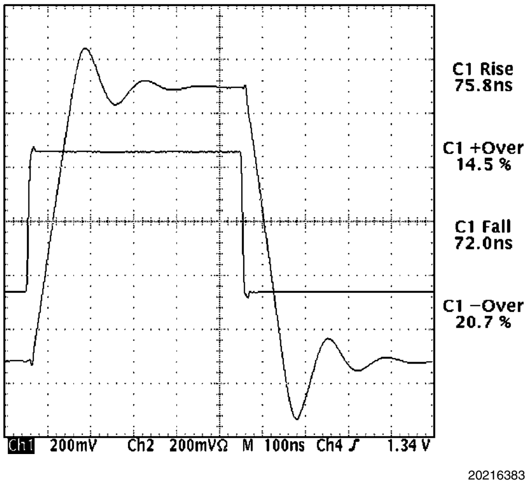


**FIGURE 12. LMV796 Response Gain = +2**

The response shown in *Figure 11* is close to the response shown in *Figure 9*. The part is actually slightly faster in the non-inverting configuration. Decreasing the value of $R_C$ to around 200Ω can decrease the negative overshoot but will have slightly longer rise and fall times. The other option is to add a small resistor in series with the input signal. *Figure 12* shows the performance of the LMV796 with no compensation. Again the decompensated parts are almost 2.5 times faster than the fully compensated op amp.

The most difficult op amp configuration to stabilize is the gain of +1. With proper compensation the LMV793/LMV794 can be used in this configuration and still maintain higher speeds than the fully compensated parts. *Figure 13* shows the gain = 1, or the buffer configuration, for these parts.

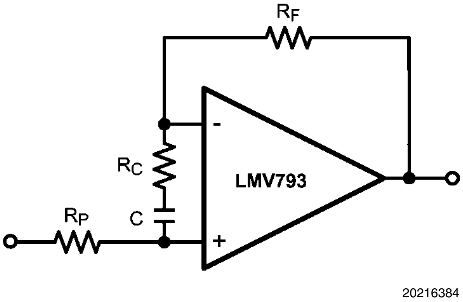


**FIGURE 13. LMV793 with Lead-Lag Compensation for Non-Inverting Configuration**

*Figure 13* is the result of using *Equation 5* and additional experimentation in the lab. $R_P$ is not part of *Equation 5*, but it is necessary to introduce another pole at the input stage for good performance at gain = +1. *Equation 5* is shown below with $R_{IN} = \infty$.

$$\left(1+\frac{R_F}{R_c}\right) = 18\text{ dB} = 7.9$$

Using 2 kΩ for $R_F$ and solving for $R_C$ gives $R_C$ = 2000/6.9 = 290Ω. The closest standard value for $R_C$ is 300Ω. After some fine tuning in the lab $R_C$ = 330Ω and $R_P$ = 1.5 kΩ were choosen as the optimum values. $R_P$ together with the input capacitance at the non-inverting pin inserts another pole into the compensation for the LMV793/LMV794. Adding this pole and slightly reducing the compensation for 1/F (using a slightly higher resistor value for $R_C$) gives the optimum response for a gain of +1. *Figure 14* is the response of the circuit shown in *Figure 13*. *Figure 15* shows the response of the LMV796 in the buffer configuration with no compensation and $R_P = R_F$ = 0.

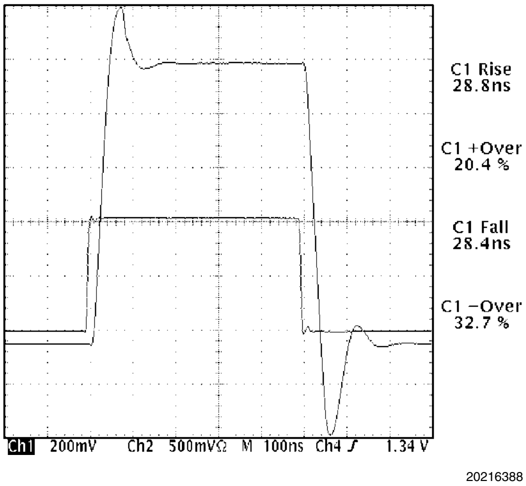
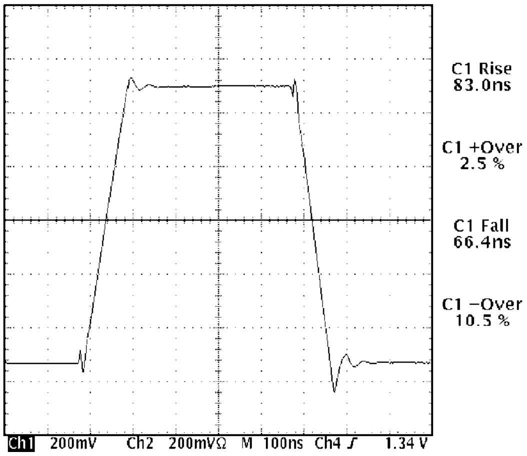


**FIGURE 14. $R_C$ = 330Ω and C = 10 nF, Gain = +1**



20216389

**FIGURE 15. LMV796 Response Gain = +1**

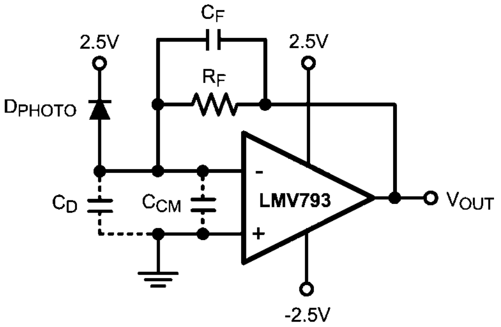
With no increase in power consumption the decompensated op amp offers faster speed over the compensated equivalent part. These examples used $R_F$ = 2 kΩ. This value is high enough to be easily driven by the LMV793/LMV794, yet small enough to minimize the effects from the parasitic capacitance of both the PCB and the op amp.

**Note:** When using the LMV793/LMV794, proper high frequency PCB layout must be followed. The GBW of these parts is 88 MHz, making the PCB layout significantly more critical than when using the compensated counterparts which have a GBW of 17 MHz.

### TRANSIMPEDANCE AMPLIFIER

An excellent application for either the LMV793 or the LMV794 is as a transimpedance amplifier. With a GBW product of 88 MHz these parts are ideal for high speed data transmission by light. The circuit shown on the front page of the datasheet is the circuit used to test the LMV793/LMV794 as transimpedance amplifiers. The only change is that VB is tied to the $V_{CC}$ of the part, thus the direction of the diode is reversed from the circuit shown on the front page.

Very high speed components were used in testing to check the limits of the LMV793/LMV794 in a transimpedance configuration. The photo diode part number is PIN-HR040 from OSI Optoelectronics. The diode capacitance for this part is only about 7 pF for the 2.5V bias used ($V_{CC}$ to virtual ground). The rise time for this diode is 1 nsec. A laser diode was used for the light source. Laser diodes have on and off times under 5 nsec. The speed of the selected optical components allowed an accurate evaluation of the LMV793 as a transimpedance amplifier. Nationals Evaluation Board for decompensated op amps, PN 551013271-001 A, was used and only minor modifications were necessary and no traces had to be cut.

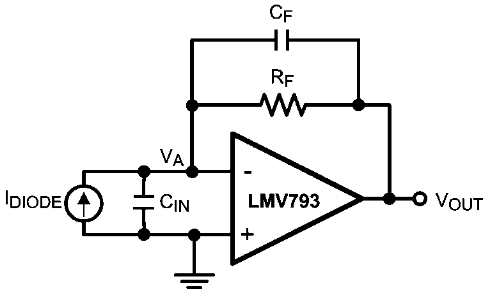


20216361

**FIGURE 16. Transimpedance Amplifier**

*Figure 16* is the complete schematic for a transimpedance amplifier. Only the supply bypass capacitors are not shown. $C_D$ represents the photo diode capacitance which is given on its datasheet. $C_{CM}$ is the input common mode capacitance of the op amp and, for the LMV793 it is shown in the last drawing of the Typical Performance Characteristics section of this datasheet. In *Figure 16* the inverting input pin of the LMV793 is kept at virtual ground. Even though the diode is connected to the 2.5V line, a power supply line is AC ground, thus $C_D$ is connected to ground.

*Figure 17* shows the schematic needed to derive F, the feedback factor, for a transimpedance amplifier. In this figure $C_D + C_{CM} = C_{IN}$. Therefore it is critical that the designer knows the diode capacitance and the op amp input capacitance. The photo diode is close to an ideal current source once its capacitance is included in the model. What kind of circuit is this? Without $C_F$ there is only an input capacitor and a feedback resistor. This circuit is a differentiator! Remember, differentiator circuits are inherently unstable and must be compensated. In this case $C_F$ compensates the circuit.



20216364

**FIGURE 17. Transimpedance Feedback Model**

Using feedback theory, $F = V_A/V_{OUT}$, this becomes a voltage divider giving the following equation:

$$F = \frac{1 + sC_F R_F}{1 + sR_F (C_F + C_{IN})}$$

The noise gain is 1/F. Because this is a differentiator circuit, a zero must be inserted. The location of the zero is given by:

$$f_z = \frac{1}{1 + sR_F (C_F + C_{IN})}$$

$C_F$ has been added for stability. The addition of this part adds a pole to the circuit. The pole is located at:

$$f_P = \frac{1}{1 + sC_F R_F}$$

To attain maximum bandwidth and still have good stability the pole is to be located on the open loop gain curve which is A. If additional compensation is required one can always increase the value of $C_F$, but this will also reduce the bandwidth of the circuit. Therefore A = 1/F, or AF = 1. For A the equation is:

$$A = \frac{\omega_{GBW}}{\omega} = \frac{f_{GBW}}{f}$$

The expression $f_{GBW}$ is the gain bandwidth product of the part. For a unity gain stable part this is the frequency where A = 1. For the LMV793 $f_{GBW}$ = 88 MHz. Multiplying A and F results in the following equation:

$$AF\Big|_{f_P} = \frac{f_{GBW}}{f} \text{ x } \frac{1 + sC_F R_F}{1 + sR_F (C_F + C_{IN})} =$$

$$\frac{f_{GBW}}{f} \text{ x } \frac{\sqrt{1 + \left(\frac{C_F R_F}{C_F R_F}\right)^2}}{\sqrt{1 + \left(\frac{R_F (C_F + C_{IN})}{C_F R_F}\right)^2}} = 1$$

For the above equation $s = j\omega$. To find the actual amplitude of the equation the square root of the square of the real and imaginary parts are calculated. At the intersection of F and A, we have:

$$\omega = \frac{1}{C_F R_F}$$

After a bit of algebraic manipulation the above equation reduces to:

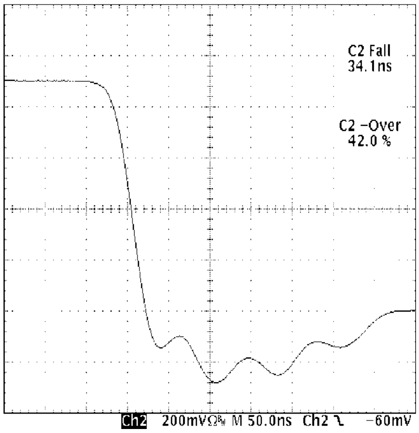
$$1 + \left(\frac{C_F + C_{IN}}{C_F}\right)^2 = 8\pi^2 f_{GBW}^2 R_F^2 C_F^2$$

In the above equation the only unknown is $C_F$. In trying to solve this equation the fourth power of $C_F$ must be dealt with. An excel spread sheet with this equation can be used and all the known values entered. Then through iteration, the value of $C_F$ when both sides are equal will be found. That is the correct value for $C_F$, and of course the closest standard value is used for $C_F$.

Before moving the lab, the transfer function of the transimpedance amplifier must be found and the units must be in Ohms.

$$V_{OUT} = \frac{-R_F}{1 + sC_F R_F} \text{ x } I_{DIODE}$$

The LMV793 was evaluated for $R_F$ = 10 kΩ and 100 kΩ, representing a somewhat lower gain configuration and with the 100 kΩ feedback resistor a fairly high gain configuration. The $R_F$ = 10 kΩ is covered first. Looking at the *Input Common Mode Capacitance vs. $V_{CM}$* chart for $C_{CM}$ for the operating point selected $C_{CM}$ = 15 pF. Note that for split supplies $V_{CM}$ = 2.5V, $C_{IN}$ = 22 pF and $f_{GBW}$ = 88 MHz. Solving for $C_F$ the calculated value is 1.75 pF, so 1.8 pF is selected for use. Checking the frequency of the pole finds that it is at 8.8 MHz, which is right at the minimum gain recommended for this part. Some over compensation was necessary for stability and the final selected value for $C_F$ is 2.7 pF. This moves the pole to 5.9 MHz. *Figure 18* and *Figure 19* show the rise and fall times obtained in the lab with a 1V output swing. The laser diode was difficult to drive due to thermal effects making the starting and ending point of the pulse quite different, therefore the two separate scope pictures.



20216390

**FIGURE 18. Fall Time**

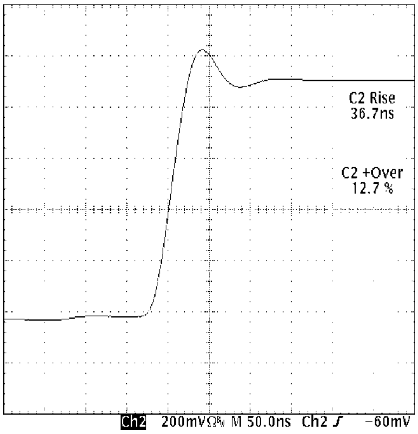


FIGURE 19. Rise Time

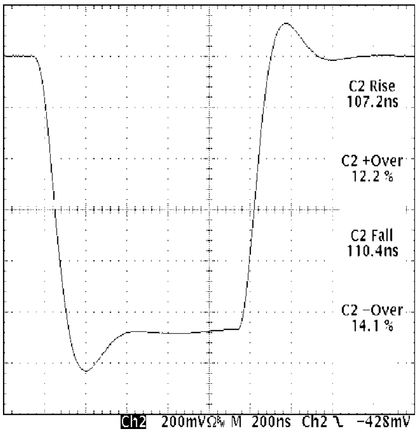


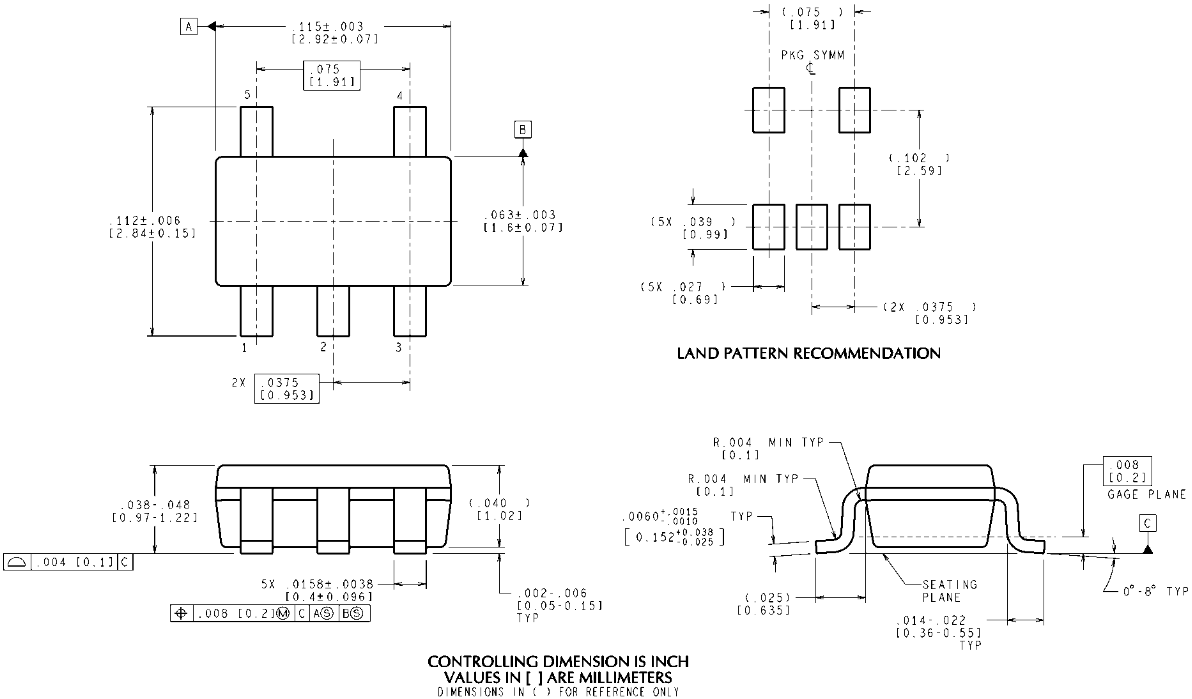
FIGURE 20. High Gain Response

In *Figure 18* the ringing and the hump during the on time is from the laser. The higher drive levels for the laser gave ringing in the light source as well as light changing from the thermal characteristics. The hump is due to the thermal characteristics.

Solving for $C_F$ using a 100 kΩ feedback resistor, the calculated value is 0.54 pF. One of the problems with more gain is the very small value for $C_F$. A 0.5 pF capacitor was used, its measured value being 0.64 pF. For the 0.64 pF location the pole is at 2.5 MHz. *Figure 20* shows the response for a 1V output.

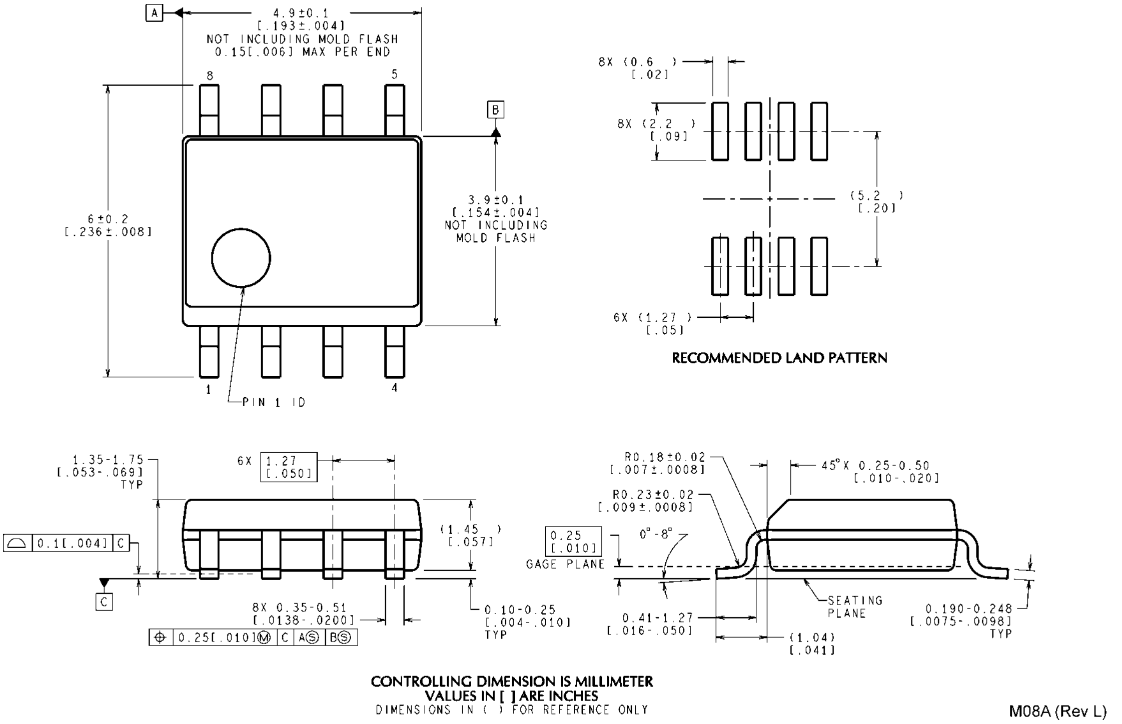
A transimpedance amplifier is an excellent application for the LMV793. Even with the high gain using a 100 kΩ feedback resistor, the bandwidth is still well over 1 MHz. Other than a little over compensation for the 10 kΩ feedback resistor configuration using the LMV793 was quite easy. Of course a very good board layout was also used for this test. For information on photo diodes please contact OSI Optoelectronics, (310) 978-0516. For further information on transimpedance amplifiers please contact your National Semiconductor representative.

## Physical Dimensions inches (millimeters) unless otherwise noted



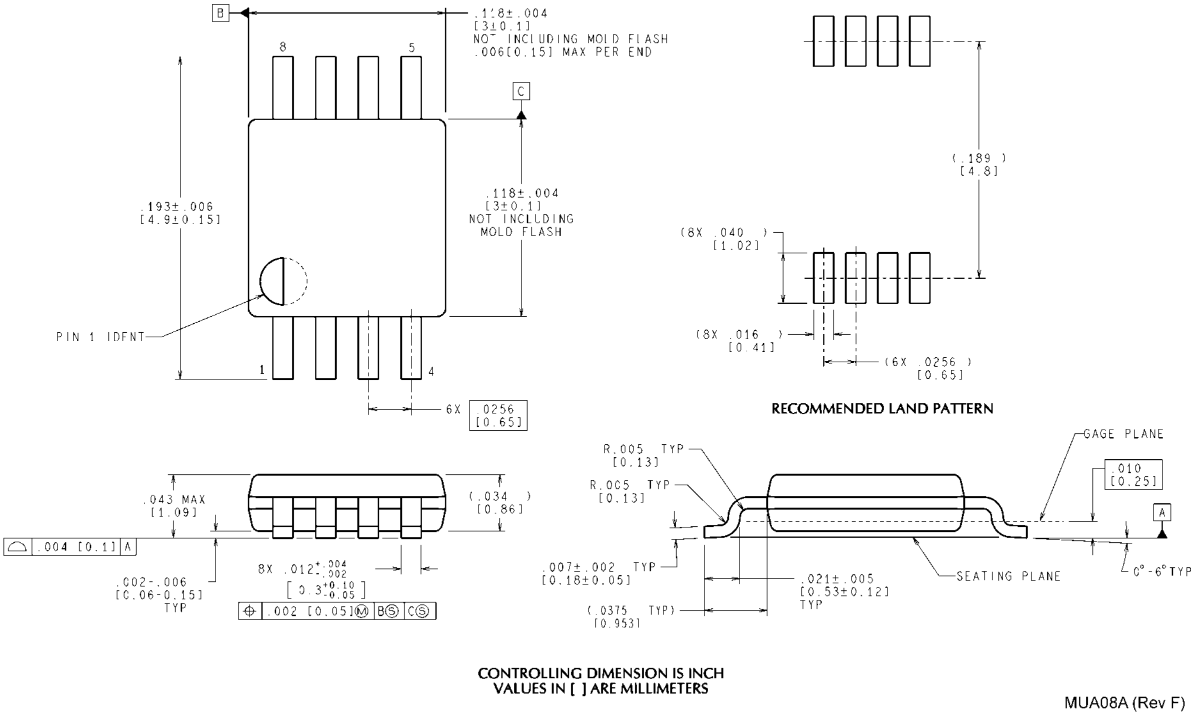
MF05A (Rev C)

**5-Pin SOT23**
**NS Package Number MF05A**



M08A (Rev L)

**8-Pin SOIC**
**NS Package Number M08A**



**8-Pin MSOP**
**NS Package Number MUA08A**

# Notes

**For more National Semiconductor product information and proven design tools, visit the following Web sites at:**

| Products | | Design Support | |
|---|---|---|---|
| Amplifiers | www.national.com/amplifiers | WEBENCH | www.national.com/webench |
| Audio | www.national.com/audio | Analog University | www.national.com/AU |
| Clock Conditioners | www.national.com/timing | App Notes | www.national.com/appnotes |
| Data Converters | www.national.com/adc | Distributors | www.national.com/contacts |
| Displays | www.national.com/displays | Green Compliance | www.national.com/quality/green |
| Ethernet | www.national.com/ethernet | Packaging | www.national.com/packaging |
| Interface | www.national.com/interface | Quality and Reliability | www.national.com/quality |
| LVDS | www.national.com/lvds | Reference Designs | www.national.com/refdesigns |
| Power Management | www.national.com/power | Feedback | www.national.com/feedback |
| Switching Regulators | www.national.com/switchers | | |
| LDOs | www.national.com/ldo | | |
| LED Lighting | www.national.com/led | | |
| PowerWise | www.national.com/powerwise | | |
| Serial Digital Interface (SDI) | www.national.com/sdi | | |
| Temperature Sensors | www.national.com/tempsensors | | |
| Wireless (PLL/VCO) | www.national.com/wireless | | |

**LIFE SUPPORT POLICY**

**NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION.** As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

For the most current product information visit us at www.national.com

**National Semiconductor**
**Americas Technical**
**Support Center**
Email: support@nsc.com
Tel: 1-800-272-9959

**National Semiconductor Europe**
**Technical Support Center**
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

**National Semiconductor Asia**
**Pacific Technical Support Center**
Email: ap.support@nsc.com

**National Semiconductor Japan**
**Technical Support Center**
Email: jpn.feedback@nsc.com